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Date: OCTOBER 11, 2005

To: EXAMINER REIS, TRAVIS M.
U.S. PATENT AND TRADEMARK OFFICE

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Client/Matter No.: DE000234 (7790/280)

of Pages: 24

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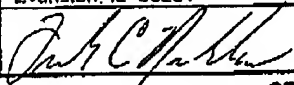
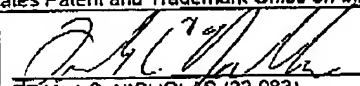
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TRANSMITTAL FORM <small>(to be used for all correspondence after initial filing)</small>	Attorney Docket No	DE000234 (7790/280)
	Application Number	10/023,168
	Filing Date	DECEMBER 18, 2001
	First Named Inventor	RALF DORSCHIED
	Group Art Unit	2859
	Examiner	REIS, TRAVIS M

ENCLOSURES (check all that apply)		
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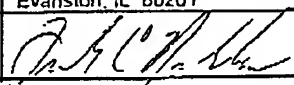
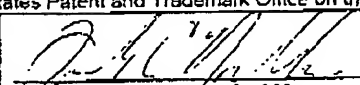
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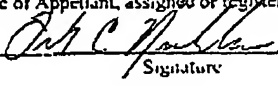
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Total		Minus		0	\$25	0	\$50	
Indep		Minus		0	\$100	0	\$200	
First Presentation of Multiple Dep. Claim					\$180		\$360	
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PATENT
Case No. DE000234
(7790/280)

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES**

In re patent application of:

RALF DORSCHIED ET AL

Serial No.: 10/023,168

Filed: DECEMBER 18, 2001

For: DETECTOR FOR THE
DETECTION OF
ELECTROMAGNETIC
RADIATION

Examiner: REIS, TRAVIS M.

Group Art Unit: 2859

APPEAL BRIEF

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Appellant herewith respectfully presents a Brief on Appeal as follows:

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1. REAL PARTY IN INTEREST

The real party in interest is the assignee of record U.S. Philips Corporation, a Delaware corporation having an office and a place of business at 1251 Avenue of the Americas, New York, NY 10020-1104.

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2. RELATED APPEALS AND INTERFERENCES

Appellant and the undersigned attorney are not aware of any other appeals or interferences which will directly affect or be directly affected by or having a bearing on the Board's decision in the pending appeal.

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3. STATUS OF CLAIMS

Claims 1-8 and 12-16 are currently pending in the application and are the claims on appeal. See, the Appendix.

Claims 9-11 have been withdrawn from consideration.

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4. STATUS OF AMENDMENTS

Appellant did not file an after final request for reconsideration under 37 C.F.R. §1.116 in response to a Final Office Action dated April 15, 2005. Previous amendments to claims 1-8 in response to a Non-Final Office Action dated May 12, 2003, have been entered into the record.

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5. SUMMARY OF THE INVENTION

As illustrated in FIG. 1, the present application provides a detector (1) having ceramic basic element (4) (e.g., aluminum oxide) and a CMOS chip (3) with an intermediate layer (2) between ceramic basis element (4) and CMOS chip (3). Intermediate layer (2) includes spacers (5) (e.g., wire) in contact with ceramic basic element (4) and CMOS chip (3), and a pair of adhesives (A1) (e.g., a fast curing epoxy resin) and (B) (e.g., a low-viscosity adhesive) adhered to ceramic basic element (4) and CMOS chip (3). *See, U.S. Patent Application Serial No. 10/023,168 on page 4, line 26 to page 5, line 22.*

As illustrated in FIG. 2, detector (1) further has a scintillator (6) with an intermediate layer between CMOS chip (3) and scintillator (6). This intermediate layer includes spacers (5) in contact with CMOS chip (3), an adhesive (A2) (e.g., a fast curing epoxy resin) adhered to a spacer (5) and scintillator (6), and adhesive (B) adhered to CMOS chip (3), scintillator (6), spacer (5) and adhesive (A2). *See, U.S. Patent Application Serial No. 10/023,168 on page 5, line 23 to page 6, line 20.*

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6. GROUND OF REJECTION TO BE REVIEWED ON APPEAL

Claims 1-4, 6-8 and 12-16 stand finally rejected under 35 U.S.C. §103(a) over U.S. Patent No. 6,292,528 to *Wieczorek* et al. in view of U.S. Patent No. 6,420,213 to *Nakajyo* et al. and in further view of U.S. Patent No. 6,265,782 to *Yamamoto* et al.

Claim 5 stands finally rejected under 35 U.S.C. §103(a) over U.S. Patent No. 6,292,528 to *Wieczorek* et al. in view of U.S. Patent No. 6,420,213 to *Nakajyo* et al. U.S. Patent No. 6,265,782 to *Yamamoto* et al. and in further view of U.S. Patent No. 6,063,688 to *Doyle* et al.

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7. ARGUMENT

Obviousness. To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. See, MPEP §2143.

Wieczorek, Nakajyo and Yamamoto Combination. The Appellant respectfully traverse the obviousness rejections of claims 1-8 and 12-16, because Examiner Reis has failed to establish a *prima facie* case of obviousness as required by MPEP §2143. Specifically, Examiner Reis has failed to cite a legally sufficient suggestion or a legally sufficient motivation, in *Wieczorek, Nakajyo* and *Yamamoto* to modify *Wieczorek* in view of *Nakajyo* and in further view of *Yamamoto* to obtain the claimed invention as recited in claims 1, 2, 4, 6 and 13-16.

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Specifically, *Wieczorek* fails to teach or suggest the following limitations of claims 1, 2, 4, 6 and 13-16:

1. "wherein said intermediate layer (2) contains at least two adhesives (A, B) of different consistency and spacers (5)" as recited in independent claim 1'
2. "wherein the gap width of the intermediate layer (2) is determined by quantities of the adhesive (A) and a plurality of spacers (5)" as recited in dependent claim 2;
3. "wherein at least some quantities of the first adhesive (A1) are applied directly to the surfaces of the CMOS chip (3) and the ceramic basic element (4) and that a plurality of spacers (5) is arranged between the surfaces of the CMOS chip (3) and the ceramic basic element (4)" as recited in dependent claim 4;

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4. "wherein at least some quantities of a second adhesive (A2) are applied to the surface of the scintillator (6) that faces the CMOS chip as well as to a plurality of bumps that are present on the CMOS chip (3)" as recited in dependent claim 6;

5. "said first intermediate layer (2) including a first spacer (5) in contact with said ceramic basic element (4) and said CMOS chip (3), a first adhesive (A1) adhered to said ceramic basic element (4) and said CMOS chip (3), and a second adhesive (B) adhered to said ceramic basic element (4) and said CMOS chip (3)" as recited in independent claim 13;

6. "wherein said second adhesive (B) is between and adhered to said first spacer (5) and said first adhesive (A1)" as recited in dependent claim 14;

7. "said second intermediate layer including a second spacer (5) in contact with said CMOS chip (3), a third adhesive (A2) adhered to said second spacer (5) and said scintillator (6), and a fourth adhesive (B) adhered to said CMOS chip (3), said scintillator (6), said second spacer (5) and said third adhesive (A2)" as recited in dependent claim 15; and

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8. "wherein said second intermediate layer further includes a third spacer (5) in contact with said CMOS chip (3)" and "wherein said fourth adhesive (B) is between and adhered to said scintillator (6) and said third spacer (5)" as recited in dependent claim 16.

Examiner Reis correctly recognizes that *Wieczorek* fails to teach the aforementioned limitations of claims 1, 2, 4, 6 and 13-16. As such, Examiner Reis asserts that it would have been obvious to one of ordinary skill in the art at the time the invention was made to add adhesives 5 and 7 and stub bumps 2 as illustrated in FIG. 2 of *Nakajyo* to adhesive layers 13 and 16 as illustrated in FIG. 2 of *Wieczorek* with the expectation of minimizing a stretch between electrical leads between a CMOS chip 9 and bond pads 17 on printed circuit board 15 as illustrated in FIG. 2 of *Wieczorek* by having electrically conduct material directly between the leads.

The Appellant traverses this assertion by Examiner Reis, because the mere fact that *Wieczorek* can be modified in view of *Nakajyo* to obtain the claimed invention as recited in claims 1, 2, 4, 6 and 13-16 does not render the resultant modification obvious unless the prior art also suggests the desirability of the combination. See, *In re Mills*, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990) (Claims were directed to an apparatus for producing an aerated cementitious composition by drawing air into the cementitious composition by driving the output pump at a capacity greater than the feed rate. The

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prior art reference taught that the feed means can be run at a variable speed, however the court found that this does not require that the output pump be run at the claimed speed so that air is drawn into the mixing chamber and is entrained in the ingredients during operation. Although a prior art device "may be capable of being modified to run the way the apparatus is claimed, there must be a suggestion or motivation in the reference to do so." 916 F.2d at 682, 16 USPQ2d at 1432.). See also *In re Fritch*, 972 F.2d 1260, 23 USPQ2d 1780 (Fed. Cir. 1992) (flexible landscape edging device which is conformable to a ground surface of varying slope not suggested by combination of prior art references).

The basis for Examiner Reis' assertion is that *Nakajyo* suggests the desirability of the combination by offering adhesives 5 and 7 and stud bumpers 2 that can be placed between scintillator 11 (FIG. 1) and CMOS chip 9 (FIG. 1) of *Wieczorek* and between CMOS chip 9 and printed circuit board 15 (FIG. 1) of *Wieczorek* in order to ensure the standard flatness between scintillator 11 and CMOS chip 9 of *Wieczorek* and between CMOS chip 9 and printed circuit board 15 of *Wieczorek* to thereby minimize the stretch between electrical leads by preventing one side to be higher than the opposite side. However, Examiner Reis CAN NOT conclusively assert that an implementation of the adhesives 5 and 7 and stud bumpers 2 of *Nakajyo* between CMOS chip 9 and bond pad 17 on printed circuit board 15 of *Wieczorek* would ensure the standard flatness between scintillator 11 and CMOS chip 9 of *Wieczorek* and between CMOS chip 9 and printed circuit board 15 of *Wieczorek* to thereby minimize the stretch between electrical leads by

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preventing one side to be higher than the opposite side. This is particularly true in view of the fact that neither *Wieczorek* nor *Nakajyo* describe an absolute minimum stretch and/or an absolute maximum stretch of the electrical leads between CMOS chip 9 and bond pad 17 on printed circuit board 15 that are conducive to reducing noise and susceptibility of interference as required by *Wieczorek* as correlated to a flatness of the various components. See, *Wieczorek* at column 2, line 43-54; and column 5, lines 13-16. Thus, one side being higher than the other does not guarantee a minimal stretch of electrical leads as asserted by Examiner Reis.

Moreover, the Appellant respectfully asserts that there is no motivation or suggestion to replace adhesive layers 13 and 16 with the adhesives and spacers of *Nakajyo* in view of the facts that (1) *Wieczorek* does not denounce adhesive layers 13 and 16 as being a less than perfect technique for bonding CMOS chip 9 and printed circuit board 15 with the goal of minimizing the stretch of electrical leads between CMOS chip 9 and bond pads 17, and (2) *Nakajyo* does not proclaim adhesives 5 and 7 and stud bumps 2 as the best technique for bonding elements (e.g., CMOS chip 9 and printed circuit board 15) with the goal of minimizing the stretch of electrical leads between the elements.

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In summary, Examiner Reis fails to provide a suggestion or a motivation to modify *Wieczorek* in view of *Nakajyo* and *Yamamoto* as proposed by Examiner Reis. Withdrawal of the rejection of claims 1-4, 6-8 and 12-16 under §103(a) as being unpatentable over *Wieczorek* in view of *Nakajyo* and *Yamamoto* and a withdrawal of the rejection of claim 5 under §103(a) as being unpatentable over *Wieczorek* in view of *Nakajyo* and *Yamamoto* and in further view of *Doyle* are therefore respectfully requested.

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Dated: October 11, 2005

Respectfully submitted,
Ralf Dorscheide, et al

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CLAIMS APPENDIX

1. A detector for a detection of electromagnetic radiation, said detector comprising:
at least one scintillator (6);
at least one CMOS chip (3); and
a ceramic basic element (4),
wherein a respective intermediate layer (2) that is defined in respect of its gap width is arranged each time between the scintillator (6) and the CMOS chip (3) and between the CMOS chip (3) and the ceramic basic element (4), and
wherein said intermediate layer (2) contains at least two adhesives (A, B) of different consistency and spacers (5).
2. The detector as claimed in claim 1, wherein the gap width of the intermediate layer (2) is determined by quantities of the adhesive (A) and a plurality of spacers (5).
3. The detector as claimed in the claims 1 and 2, wherein a first adhesive (A) is a fast curing epoxy resin, cyanoacrylate or acrylate adhesive.

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4. The detector as claimed in claim 3, wherein at least some quantities of the first adhesive (A1) are applied directly to the surfaces of the CMOS chip (3) and the ceramic basic element (4) and that a plurality of spacers (5) is arranged between the surfaces of the CMOS chip (3) and the ceramic basic element (4).
5. The detector as claimed in claim 4, wherein each spacer (5) is a wire that consists notably of the materials Au and AlSi.
6. The detector as claimed in claim 3, wherein at least some quantities of a second adhesive (A2) are applied to the surface of the scintillator (6) that faces the CMOS chip as well as to a plurality of bumps that are present on the CMOS chip (3).
7. The detector as claimed in claim 1, wherein a first adhesive (B) is a low-viscosity adhesive, notably on an epoxy resin basis.
8. The detector as claimed in claim 1, wherein the ceramic basic element (4) is based on aluminum oxide.
12. An X-ray examination apparatus that includes at least one detector as claimed in one of the claims 1 to 8.

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13. A detector for detecting electromagnetic radiation, said detector comprising:
- a ceramic basic element (4);
 - a CMOS chip (3); and
 - a first intermediate layer (2) between said ceramic basis element (4) and said CMOS chip (3), said first intermediate layer (2) including
 - a first spacer (5) in contact with said ceramic basic element (4) and said CMOS chip (3),
 - a first adhesive (A1) adhered to said ceramic basic element (4) and said CMOS chip (3), and
 - a second adhesive (B) adhered to said ceramic basic element (4) and said CMOS chip (3).
14. The detector of claim 13,
- wherein said second adhesive (B) is between and adhered to said first spacer (5) and said first adhesive (A1).

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15. The detector for detecting electromagnetic radiation of claim 13, further comprising:

a scintillator (6); and

a second intermediate layer between said CMOS chip (3) and said scintillator (6),

said second intermediate layer including

a second spacer (5) in contact with said CMOS chip (3),

a third adhesive (A2) adhered to said second spacer (5) and said

scintillator (6), and

a fourth adhesive (B) adhered to said CMOS chip (3), said scintillator (6),

said second spacer (5) and said third adhesive (A2).

16. The detector of claim 15,

wherein said second intermediate layer further includes a third spacer (5) in contact with said CMOS chip (3); and

wherein said fourth adhesive (B) is between and adhered to said scintillator (6) and said third spacer (5).

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EVIDENCE APPENDIX

None.

RELATED PROCEEDINGS APPENDIX

None.